In the Claims:

Please amend the claims as follows:

1. (Previously Presented) A non-volatile memory cell integrated on a semiconductor substrate and comprising:

a floating gate transistor including a source region and a drain region, a gate region projecting from the substrate and comprised between said source and drain regions, said gate region having a predetermined length and width and comprising a first floating gate region and a control gate region, wherein said floating gate region is insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions, by a dielectric layer with low dielectric constant value.

2. (Previously Presented) A memory cell according to claim 1, wherein said floating gate regions are covered by a dielectric layer before being insulated from each other through said dielectric layer with low dielectric constant value.

3. (Previously Presented) A memory cell according to claim 1, wherein said dielectric layer with low dielectric constant value is bounded between said floating gate regions.

4. (Previously Presented) A memory cell according to claim 1, wherein said dielectric layer with low dielectric constant value is formed by a layer of material having a dielectric constant comprised between 1 and 3.9.

5. (Previously Presented) A memory cell according to claim 1, wherein said dielectric layer with low dielectric constant value is formed by a silicon oxide layer doped with fluorine.

6. (Original) A memory cell according to claim 1, wherein said dielectric layer with low dielectric constant value is formed by a carbon oxide layer hydrated with alkylic groups.

7-14. (Cancelled)

15. (Previously Presented) A memory cell matrix formed on a semiconductor substrate comprising a plurality of memory cells organized in rows and columns, each cell in a given row being coupled to a corresponding word line and each cell being formed according to claim 1, the cell matrix being wherein adjacent memory cells being coupled to a same word line of said memory cell matrix are insulated from each other by a dielectric layer with low dielectric constant value.

16. (Currently Amended) A memory-cell structure formed on a semiconductor substrate, the memory-cell structure comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell in a respective row being coupled to a corresponding word line and each memory cell including a floating gate region, the memory-cell structure including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of the memory cells in a row that are coupled to the same word line.

17. (Original) The memory-cell structure of claim 16 further comprising a dielectric layer having a greater dielectric constant than the insulating regions formed on the floating gate regions.

18. (Original) The memory-cell structure of claim 16 wherein the insulating layer has a dielectric constant having a value of between approximately 1 and approximately 3.9.

19. (Original) The memory-cell structure of claim 16 each memory cell further comprises a control gate region capacitively coupled to the floating gate region through a dielectric layer having a dielectric constant greater than that of the insulating layer, and wherein the control gate regions of memory cells in respective rows are electrically interconnected.

20. (Original) The memory-cell structure of claim 16 wherein each memory cell comprises a FLASH memory cell.

21. (Currently Amended) A memory device, comprising:

a memory-cell array formed on a semiconductor substrate, the memory-cell array comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell in a respective row being coupled to a corresponding word line and each memory cell including a floating gate region, the memory-cell array including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of the memory cells in a row that are coupled to the same word line.

22. (Original) The memory device of claim 21 wherein the memory device comprises a FLASH memory device and each memory cell comprises a FLASH memory cell.

23. (Original) The memory device of claim 21 further comprising a dielectric layer having a greater dielectric constant than the insulating regions formed on the floating gate regions.

24. (Currently Amended) An electronic system, comprising:

a memory device including,

a memory-cell array formed on a semiconductor substrate, the memory-cell array comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell in a respective row being coupled to a corresponding word line and each memory cell and including a floating gate region, the memory-cell array including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of the memory cells in a row that are coupled to the same word line.

25. (Original) The electronic system of claim 24 wherein the electronic system comprises a computer system.

26. (Original) The electronic system of claim 25 wherein the memory device comprises a FLASH memory device and each memory cell comprises a FLASH memory cell.

27-30. (Cancelled)

31. (Currently Amended) A memory-cell structure formed on a semiconductor substrate, the memory-cell structure comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell in a respective row being coupled to a corresponding word line and each memory cell including a gate structure having a floating gate region and a control gate region, the memory-cell structure including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of the memory cells in a row that are coupled to the same word line, the insulating region having a first side in direct contact with a first one of the adjacent floating gate regions and a second side in direct contact with a second one of the adjacent floating gate regions.

32. (Previously Presented) The memory-cell structure of claim 31 further comprising a dielectric layer having a greater dielectric constant than the insulating region formed between adjacent floating gate regions, the dielectric layer being formed on the insulating region and on the floating gate regions.

33. (Previously Presented) The memory-cell structure of claim 32 wherein the insulating region has a dielectric constant having a value of between approximately 1 and approximately 3.9.

34. (Previously Presented) The memory-cell structure of claim 31 wherein each memory cell comprises a FLASH memory cell.

35. (New) The memory-cell matrix of claim 15 wherein the dielectric layer completely fills a space between adjacent memory cells coupled to the same word line.

36. (New) The memory-cell structure of claim 16 wherein the dielectric layer completely fills a space between adjacent memory cells coupled to the same word line.

37. (New) The memory device of claim 21 wherein the dielectric layer completely fills a

space between adjacent memory cells coupled to the same word line.

38. (New) The electronic system of claim 24 wherein the dielectric layer completely fills a space between adjacent memory cells coupled to the same word line.